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09/783,626	02/14/2001	Mark Kaplun	100.004US01	2709

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EXAMINER	
TRAN, QUOC DUC	

ART UNIT	PAPER NUMBER
2643	16

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/783,626	Applicant(s) KAPLUN ET AL.
	Examiner Quoc D Tran	Art Unit 2643

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

RESPONSE

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-22, 24-26 and 30-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Tyburski et al (5,495,470).

Consider claim 1, Tyburski et al teach an alarm mechanism, comprising: a hardware component, including first and second registers, the first register adapted to store a value that indicates a change in state of at least one alarm and the second register adapted to store current states of each of the at least one alarm; and a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers (col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 14 lines 19-38; col. 20 lines 22-36).

Consider claim 2, Tyburski et al teach wherein the first and second registers comprise first and second n-bit registers for monitoring n alarms (col. 20 lines 22-36).

Consider claim 3, Tyburski et al teach the alarm mechanism and further including a monitoring circuit adapted to monitor serial lines on the backplane of an access device of a telecommunications network to detect alarm conditions and to report alarm conditions to the hardware component (col. 13 line 55 – col. 14 line 7; col. 14 line 61 – col. 15 line 45).

Consider claim 4, Tyburski et al teach wherein the second register is adapted to store a first value for a first state and second value for a second state (col. 23 line 50 – col. 24 line 51).

Consider claim 5, Tyburski et al teach wherein the second register is adapted to store a first logic value for an alarm state and a second logic value for a non-alarm state (col. 18 line 37 – col. 19 line 10).

Consider claim 6, Tyburski et al teach wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm indicator (col. 23 line 50 – col. 24 line 51).

Consider claim 7, Tyburski et al teach an alarm mechanism, comprising: at least one alarm; a first register, responsive to the at least one alarm, and adapted to store a value that indicates a change in state of at least one alarm; and a second register, responsive to the at least one alarm, and adapted to store current states of each of the at least one alarm (col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 14 lines 19-38; col. 20 lines 22-36).

Consider claim 8, Tyburski et al teach wherein the at least one alarm comprises an alarm for a serial line on the backplane of an access device (col. 13 line 55 – col. 14 line 7; col. 14 line 61 – col. 15 line 45).

Consider claim 9, Tyburski et al teach wherein the first and second registers comprise first and second n-bit registers for monitoring n alarms (col. 20 lines 22-36).

Consider claim 10, Tyburski et al teach the alarm mechanism further including a monitoring circuit adapted to monitor serial lines on the backplane of an access device of a telecommunications network to detect alarm conditions and to report alarm conditions to the hardware component (col. 13 line 55 – col. 14 line 7; col. 14 line 61 – col. 15 line 45).

Consider claim 11, Tyburski et al teach wherein the second register is adapted to store a first value for a first state and a second value for a second state (col. 23 line 50 – col. 24 line 51).

Consider claim 12, Tyburski et al teach wherein the second register is adapted to store a first logic value for an alarm state and a second logic value for a non-alarm state (col. 18 line 37 – col. 19 line 10).

Consider claim 13, Tyburski et al teach wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm indicator (col. 23 line 50 – col. 24 line 51).

Consider claim 14, Tyburski et al teach a method for monitoring alarm conditions, the method comprising: receiving an indication of a change in state of an alarm; recording the change in state of the alarm in a first register; recording the current state of the changed alarm in a second register; and generating an interrupt (col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 14 lines 19-38; col. 20 lines 22-36).

Consider claim 15, Tyburski et al teach wherein receiving an indication of a change in state of an alarm comprises receiving an indication of an alarm condition in a serial line on a backplane of an access device (col. 13 line 55 – col. 14 line 7; col. 14 line 61 – col. 15 line 45).

Consider claim 16, Tyburski et al teach wherein recording the change in state comprises recording a first logic value in a bit location of the first register (col. 23 line 50 – col. 24 line 51).

Consider claim 17, Tyburski et al teach wherein recording the current state comprises recording a first logic value in a bit location of the second register (col. 23 line 50 – col. 24 line 51).

Consider claim 18, Tyburski et al teach wherein receiving an indication of a change in state of an alarm comprises receiving an indication of an alarm condition when at least two cells are received on communication line with corrupted synchronization patterns (col. 24 lines 40-51).

Consider claim 19, Tyburski et al teach a telecommunications system, comprising: at least one access device having a plurality of ports adapted to couple to a plurality of subscriber lines; a plurality of line cards disposed in the at least one access device and providing the plurality of ports; a monitoring circuit disposed in the access device, the monitoring circuit adapted to monitor for alarm conditions for the at least one access device; and an alarm mechanism, communicatively coupled to the monitoring circuit (col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 14 lines 19-38), the alarm mechanism including: a hardware component, including first and second registers, the first register adapted to store a value that indicates a change in state of at least one alarm and the second register adapted to store current states of each of the at least one alarm, and a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers (col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 14 lines 19-38; col. 20 lines 22-36).

Consider claim 20, Tyburski et al teach wherein the access device comprises a multimedia channel bank (col. 2 lines 37-48).

Consider claim 21, Tyburski et al teach wherein the access device comprises a digital loop carrier (col. 2 lines 29-63; col. 7 lines 29-59).

Consider claim 22, Tyburski et al teach wherein the monitoring circuit comprises a monitoring circuit that monitors serial lines on the backplane of the access device (col. 13 line 55 – col. 14 line 7; col. 14 line 61 – col. 15 line 45).

Consider claim 24, Tyburski et al teach wherein the first and second registers comprise first and second n-bit registers (col. 20 lines 22-36).

Consider claim 25, Tyburski et al teach wherein the second register is adapted to store a first logic value for an alarm state and a second logic value for a non-alarm state (col. 18 line 37 – col. 19 line 10).

Consider claim 26, Tyburski et al teach wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm (col. 23 line 50 – col. 24 line 51).

Consider claim 30, Tyburski et al teach a method for monitoring alarm conditions in an access device, the method comprising: monitoring a plurality of serial lines on a backplane of the access device (col. 13 line 55 – col. 14 line 7; col. 14 line 61 – col. 15 line 45); when successive cells have corrupted synchronization patterns, generating an alarm; receiving the alarm; recording a change in state of an alarm in a first n-bit register; recording the current state of the changed alarm in a second n-bit register; and generating an interrupt for a software component to read the first and second n-bit registers (col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 14 lines 19-38; col. 20 lines 22-36).

Consider claim 31, Tyburski et al teach wherein receiving an alarm indicator comprises receiving an indication of an alarm condition in a serial line on the backplane of an access device (col. 13 line 55 – col. 14 line 7; col. 14 line 61 – col. 15 line 45).

Consider claim 32, Tyburski et al teach wherein recording a change in state comprises recording a first logic value in a bit location of the first n-bit register (col. 23 line 50 – col. 24 line 51).

Consider claim 33, Tyburski et al teach wherein recording the current state comprises recording a first logic value in a bit location of the second n-bit register (col. 23 line 50 – col. 24 line 51).

Consider claim 34, Tyburski et al teach wherein receiving the alarm comprises receiving an indication of an alarm condition when at least two cells are received on communication line with corrupted synchronization patterns (col. 24 lines 40-51).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tyburski et al (5,495,470) in view of Gradl et al (6,381,269).

Consider claim 27, Tyburski et al teach an alarm mechanism for a telecommunications access device, comprising: at least one alarm associated with each of a plurality of serial lines of the access device; a first n-bit register, responsive to the at least one alarm and adapted to store a value that indicates a change in state of the at least one alarm; a second n-bit register, responsive to the at least one alarm, and adapted to store current states of each of the at least one alarm; and wherein corresponding bits of the first and second n-bit registers are associated with a

corresponding alarm and a corresponding line (col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 14 lines 19-38; col. 20 lines 22-36).

Tyburski et al did not clearly suggest wherein serial lines are of low voltage differential signal (LVDS) lines of the access device. However, Gradl et al suggested such (col. 1 lines 18-25; col. 3 line 50-61; col. 4 lines 37-65).

Therefore, it would have been obvious to one if the ordinary skill in the art at the time the invention was made to utilize the teaching of Gradl et al into view of Tyburski et al in order to provide synchronization signal to the backplane and to reduce signal interference.

Consider claim 28, Tyburski et al teach wherein the second register is adapted to store a first logic value for an alarm state and a second logic value for a non-alarm state (col. 18 line 37 – col. 19 line 10).

Consider claim 29, Tyburski et al teach wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm indicator (col. 23 line 50 – col. 24 line 51).

5. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tyburski et al (5,495,470) in view of Anand (5,426,688).

Consider claim 23, Tyburski et al suggest wherein the line cards comprise at least one of Plain Old Fashion Telephone Service (POTS) and digital subscriber line (DSL) (col. 7 line 29 – col. 8 line 52). Tyburski et al did not clearly suggest wherein the line cards comprise at least one of Integrated Services Digital Network (ISDN). However, Anand suggested such (col. 1 lines 6-29; col. 2 lines 10-32; col. 6 line 55 – col. 7 line 24). Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the teaching

of Anand into view of Tyburski et al in order to provide monitoring in a boarder range of telephone, data and services.

Response to Arguments

6. Applicant's arguments filed 5/5/2003 have been fully considered but they are not persuasive.

Regarding applicant's argument that Tyburski does not teach or suggest an alarm mechanism including a hardware component, including first and second registers, the first register adapted to store a value that indicates a change in state of at least one alarm and the second register adapted to store current states of each of the at least one alarm; and a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers.

Accordingly, the examiner respectfully disagrees with applicant's argument. Tyburski et al teach an alarm correlation for a telephone network (see title). The system monitors both the software and hardware functionality and report the severity of various errors found. Tyburski et al recited, "The access system…continuous non-intrusive ***performance monitoring*** of DS3 and embedded DS1 channels; non-intrusive ***performance monitoring*** of DS0 and…intrusive or non-intrusive testing of DS1, DS0 and subrate channels; and an ***OS interface for reporting and control***. In general, the ***performance monitoring function stores notable events and calculates statistics such as error rates.*** Among others, the parameters and events ***monitored at the DS3 level by the access system*** 170 include: frame format, bipolar violations (BPV) and loss of signal (LOS). DS3 level statistics, including, for example, ***frame format status, F bit error count and frame parity error count, are stored and reported to the OS***. Similarly, DS1 level ***performance***

monitoring and statistics, and TAD/FAD performance monitoring are stored in memory by the system 170. ***The access system*** 170 integrates monitor, access, and test functions into one system having ***three shelves of hardware***...The access system 170 is modular in design, supporting the network as it expands and enabling easy integration of hardware and software capabilities. ***Each hardware module contains a processor complex***...that provides data collection, control, and communication to the central administration processor 190. The Administration Shelf 200 contains the ***central computing elements and memory storage resources***...The Administration Shelf 200 is the source of system generated office alarms including audible, visual, and telemetry, as well as displays...The Office Alarm Interface Module 214 generates audible 216a, visual 216b, and telemetry 216c ***alarms for critical, major, and minor office alarms***...Every ten ms, the DS3 Module 68000 ***processor reads a sixteen bit word from the FDL uC 254***. The sixteen bit words contain the extracted FDL messages along with header information to identify the DS1 channel, the message type (scheduled/unscheduled), and the 8052 ***internal buffer status***...The interface between the 68000 and the 8052 is implemented with ***two 8-bit tri-state buffers and an 8-bit register***...a watchdog low speed clock signal is sent from the uC to the 68000 to provide an ***indication of sanity***...***The software for the access system*** 170 also comprises ***a performance monitoring (PM) process 393 which is periodically executed in the DS3 interface*** 171 (FIG. 4). The process 393 begins at state 394 by ***reading performance monitoring (PM) registers located inside of the DAI circuit 250***. ***PM statistics are accumulated and stored in on-board semiconductor memory at state 395***. Moving to state 396, the statistics are tested for whether any thresholds have been exceeded. ***If a threshold has been exceeded, an alarm/event message is constructed at state 397, forwarded to***

the administration processor 190, and sent back to the OS...***If no threshold is reached, or the alarm/event message has been sent, the PM process 393 terminates***. As indicated by state 398, once a PM interval expires, the PM process 393 is restarted" (see col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 14 lines 19-38; col. 20 lines 22-36). Therefore, Tyburski et al clearly read on the claim limitation of applicant alarm mechanism as presented in the claim.

Regarding applicant's argument that Tyburski does not teach or suggest an alarm mechanism, including at least one alarm; a first register, responsive to the at least one alarm, and adapted to store a value that indicates a change in state of at least one alarm; and a second register, responsive to the at least one alarm, and adapted to store current states of each of the at least one alarm.

Accordingly, the examiner respectfully disagrees with applicant's argument. Tyburski et al teach an alarm correlation for a telephone network (see title). The system monitors both the software and hardware functionality and report the severity of various errors found. Tyburski et al recited, "The access system...continuous non-intrusive ***performance monitoring*** of DS3 and embedded DS1 channels; non-intrusive ***performance monitoring*** of DS0 and...intrusive or non-intrusive testing of DS1, DS0 and subrate channels; and an ***OS interface for reporting and control***. In general, the ***performance monitoring function stores notable events and calculates statistics such as error rates.*** Among others, the parameters and events ***monitored at the DS3 level by the access system*** 170 include: frame format, bipolar violations (BPV) and loss of signal (LOS). DS3 level statistics, including, for example, ***frame format status, F bit error count and frame parity error count, are stored and reported to the OS***. Similarly, DS1 level ***performance monitoring and statistics, and TAD/FAD performance monitoring are stored in memory by the***

system 170. ***The access system*** 170 integrates monitor, access, and test functions into one system having ***three shelves of hardware***...The access system 170 is modular in design, supporting the network as it expands and enabling easy integration of hardware and software capabilities. ***Each hardware module contains a processor complex***...that provides data collection, control, and communication to the central administration processor 190. The Administration Shelf 200 contains the ***central computing elements and memory storage resources***...The Administration Shelf 200 is the source of system generated office alarms including audible, visual, and telemetry, as well as displays...The Office Alarm Interface Module 214 generates audible 216a, visual 216b, and telemetry 216c ***alarms for critical, major, and minor office alarms***...Every ten ms, the DS3 Module 68000 ***processor reads a sixteen bit word from the FDL uC 254***. The sixteen bit words contain the extracted FDL messages along with header information to identify the DS1 channel, the message type (scheduled/unscheduled), and the 8052 ***internal buffer status***...The interface between the 68000 and the 8052 is implemented with ***two 8-bit tri-state buffers and an 8-bit register***...a watchdog low speed clock signal is sent from the uC to the 68000 to provide an ***indication of sanity***...***The software for the access system*** 170 also comprises ***a performance monitoring (PM) process 393 which is periodically executed in the DS3 interface*** 171 (FIG. 4). The process 393 begins at state 394 by ***reading performance monitoring (PM) registers located inside of the DAI circuit 250***. ***PM statistics are accumulated and stored in on-board semiconductor memory at state 395***. Moving to state 396, the statistics are tested for whether any thresholds have been exceeded. ***If a threshold has been exceeded, an alarm/event message is constructed at state 397, forwarded to the administration processor 190, and sent back to the OS***...***If no threshold is reached, or the***

alarm/event message has been sent, the PM process 393 terminates. As indicated by state 398, once a PM interval expires, the PM process 393 is restarted" (see col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 14 lines 19-38; col. 20 lines 22-36). Therefore, Tyburski et al clearly read on the claim limitation of applicant alarm mechanism as presented in the claim.

Applicant goes on with similar arguments as discussed above with respect to claim 14 and 19. Therefore, the response will be similar to the above.

Regarding applicant's argument that Tyburski does not teach or suggest a method of monitoring alarm condition in an access device including monitoring a plurality of serial lines on a backplane of the access device; when successive cells have corrupted synchronization patterns, generating an alarm; receiving the alarm; recording a change in state of an alarm in a first n-bit register; recording the current state of the changed alarm in a second n-bit register; and generating an interrupt for a software component to read the first and second n-bit registers.

Accordingly, the examiner respectfully disagrees with applicant's argument. Tyburski et al teach an alarm correlation for a telephone network for provides an integrated approach to synchronization measurement and relative synchronization, and also provides alarm correlation and hierarchical event filtering. The system monitors both the software and hardware functionality and report the severity of various errors found. Tyburski et al recited, "The access system…continuous non-intrusive ***performance monitoring*** of DS3 and embedded DS1 channels; non-intrusive ***performance monitoring*** of DS0 and…intrusive or non-intrusive testing of DS1, DS0 and subrate channels; and an ***OS interface for reporting and control***. In general, the ***performance monitoring function stores notable events and calculates statistics such as error rates.*** Among others, the parameters and events ***monitored at the DS3 level by the access***

system 170 include: frame format, bipolar violations (BPV) and loss of signal (LOS). DS3 level statistics, including, for example, ***frame format status, F bit error count and frame parity error count, are stored and reported to the OS***. Similarly, DS1 level ***performance monitoring and statistics, and TAD/FAD performance monitoring are stored in memory by the system 170***. ***The access system*** 170 integrates monitor, access, and test functions into one system having ***three shelves of hardware***...The access system 170 is modular in design, supporting the network as it expands and enabling easy integration of hardware and software capabilities. ***Each hardware module contains a processor complex***...that provides data collection, control, and communication to the central administration processor 190. The Administration Shelf 200 contains the ***central computing elements and memory storage resources***...The Administration Shelf 200 is the source of system generated office alarms including audible, visual, and telemetry, as well as displays...The Office Alarm Interface Module 214 generates audible 216a, visual 216b, and telemetry 216c ***alarms for critical, major, and minor office alarms***...Every ten ms, the DS3 Module 68000 ***processor reads a sixteen bit word from the FDL uC 254***. The sixteen bit words contain the extracted FDL messages along with header information to identify the DS1 channel, the message type (scheduled/unscheduled), and the 8052 ***internal buffer status***...The interface between the 68000 and the 8052 is implemented with ***two 8-bit tri-state buffers and an 8-bit register***...a watchdog low speed clock signal is sent from the uC to the 68000 to provide an ***indication of sanity...A crosspoint switch array 278 is provided as the interface between the DAI 250 and the DS2 links 282 on the backplane***. In this manner any of the seven DS2 signals from the DAI 250 can be connected to any of the seven DS2 links 282 on the backplane...the DS2 data coming from the DAI 250 is fed through inverting buffers 280 and

out onto the backplane. Both the DS2 clock and frame signals coming from the DAI 250 are sent through 7x7 crosspoint arrays 278 and fed through non-inverting buffers 280' (not shown) and out to the backplane...***The software for the access system*** 170 also comprises ***a performance monitoring (PM) process 393 which is periodically executed in the DS3 interface*** 171 (FIG. 4). The process 393 begins at state 394 by ***reading performance monitoring (PM) registers located inside of the DAI circuit 250***. ***PM statistics are accumulated and stored in on-board semiconductor memory at state 395***. Moving to state 396, the statistics are tested for whether any thresholds have been exceeded. ***If a threshold has been exceeded, an alarm/event message is constructed at state 397, forwarded to the administration processor 190, and sent back to the OS***...***If no threshold is reached, or the alarm/event message has been sent, the PM process 393 terminates***. As indicated by state 398, once a PM interval expires, the PM process 393 is restarted" (see col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 13 line 55 – col. 14 line 7; col. 14 lines 19-38; col. 14 line 61 – col. 15 line 45; col. 20 lines 22-36). Therefore, Tyburski et al clearly read on the claim limitation of applicant alarm mechanism as presented in the claim.

Regarding applicant's argument that neither Tyburski nor Gradl teach or suggest an alarm mechanism including at least one alarm associated with each of a plurality of low voltage differential signal lines of the access device; a first n-bit register, responsive to the at least one alarm and adapted to store a value that indicates a change in state of the at least one alarm; a second n-bit register, responsive to the at least one alarm, and adapted to store current states of each of the at least one alarm.

Accordingly, the examiner respectfully disagrees with applicant's argument. Tyburski et al teach an alarm correlation for a telephone network for provides an integrated approach to

synchronization measurement and relative synchronization, and also provides alarm correlation and hierarchical event filtering. The system monitors both the software and hardware functionality and report the severity of various errors found. Tyburski et al recited, "The access system...continuous non-intrusive ***performance monitoring*** of DS3 and embedded DS1 channels; non-intrusive ***performance monitoring*** of DS0 and...intrusive or non-intrusive testing of DS1, DS0 and subrate channels; and an ***OS interface for reporting and control***. In general, the ***performance monitoring function stores notable events and calculates statistics such as error rates.*** Among others, the parameters and events ***monitored at the DS3 level by the access system*** 170 include: frame format, bipolar violations (BPV) and loss of signal (LOS). DS3 level statistics, including, for example, ***frame format status, F bit error count and frame parity error count, are stored and reported to the OS***. Similarly, DS1 level ***performance monitoring and statistics, and TAD/FAD performance monitoring are stored in memory by the system 170***. ***The access system*** 170 integrates monitor, access, and test functions into one system having ***three shelves of hardware***...The access system 170 is modular in design, supporting the network as it expands and enabling easy integration of hardware and software capabilities. ***Each hardware module contains a processor complex***...that provides data collection, control, and communication to the central administration processor 190. The Administration Shelf 200 contains the ***central computing elements and memory storage resources***...The Administration Shelf 200 is the source of system generated office alarms including audible, visual, and telemetry, as well as displays...The Office Alarm Interface Module 214 generates audible 216a, visual 216b, and telemetry 216c ***alarms for critical, major, and minor office alarms***...Every ten ms, the DS3 Module 68000 ***processor reads a sixteen bit word from the FDL uC 254***. The

sixteen bit words contain the extracted FDL messages along with header information to identify the DS1 channel, the message type (scheduled/unscheduled), and the 8052 ***internal buffer status***...The interface between the 68000 and the 8052 is implemented with ***two 8-bit tri-state buffers and an 8-bit register***...a watchdog low speed clock signal is sent from the uC to the 68000 to provide an ***indication of sanity***...***A crosspoint switch array 278 is provided as the interface between the DAI 250 and the DS2 links 282 on the backplane.*** In this manner any of the seven DS2 signals from the DAI 250 can be connected to any of the seven DS2 links 282 on the backplane...the DS2 data coming from the DAI 250 is fed through inverting buffers 280 and out onto the backplane. Both the DS2 clock and frame signals coming from the DAI 250 are sent through 7x7 crosspoint arrays 278 and fed through non-inverting buffers 280' (not shown) and out to the backplane...***The software for the access system*** 170 also comprises ***a performance monitoring (PM) process 393 which is periodically executed in the DS3 interface*** 171 (FIG. 4). The process 393 begins at state 394 by ***reading performance monitoring (PM) registers located inside of the DAI circuit 250***. ***PM statistics are accumulated and stored in on-board semiconductor memory at state 395***. Moving to state 396, the statistics are tested for whether any thresholds have been exceeded. ***If a threshold has been exceeded, an alarm/event message is constructed at state 397, forwarded to the administration processor 190, and sent back to the OS***...***If no threshold is reached, or the alarm/event message has been sent, the PM process 393 terminates***. As indicated by state 398, once a PM interval expires, the PM process 393 is restarted" (see col. 8 lines 30-52; col. 9 line 56 – col. 11 line 43; col. 13 line 55 – col. 14 line 7; col. 14 lines 19-38; col. 14 line 61 – col. 15 line 45; col. 20 lines 22-36).

Whereas, Gradl et al teach a system for evaluating a digital signal link for interference tolerance wherein the digital signal links carrying both common mode and differential mode signals (see col. 1 lines 18-25; col. 3 line 50-61; col. 4 lines 37-65). Therefore, it would have been obvious to one if the ordinary skill in the art at the time the invention was made to utilize the teaching of Gradl et al into view of Tyburski et al in order to provide synchronization signal to the backplane and to reduce signal interference. Thus, the combination of Tyburski et al and Gradl et al read on applicant's limitations as claimed.

For the reasons set forth above, claims 1-34 remain rejected either singly under Tyburski et al or in combination under Tyburski et al in view of Gradl et al.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Facsimile responses should be faxed to:

(703) 872-9314

Hand-delivered responses should be brought to:

Crystal Park II, 2121 Crystal Drive
Arlington. VA., Sixth Floor (Receptionist)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Quoc Tran** whose telephone number is **(703) 306-5643**. The examiner can normally be reached on Monday-Thursday from 8:00 to 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Curtis Kuntz**, can be reached on **(703) 305-4708**.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **Technology Center 2600** whose telephone number is **(703) 306-0377**.

July 15, 2003

CURTIS KUNTZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600